What is claimed is:

1. A method comprising:

accessing a control register mask;

adjusting a control value for a control register as a function of said control register mask to generate a masked control value;

programming said masked control value into the control register.

2. The method of claim 1 wherein said accessing comprises writing an initial value to at least one address within a memory image.

3. The method of claim 2 wherein said accessing further comprises executing a state save operation.

4. The method of claim 3 wherein said accessing further comprises comparing a saved value to said initial value, said saved value being stored within said memory image as a result of said execution of said state save operation.

5. The method of claim 4 wherein said control register mask comprises a default value if said saved value is equal to said initial value.

6. The method of claim 5 wherein said control register mask comprises said saved value if said saved value is not equal to said initializing value.

7. The method of claim 6 wherein said adjusting comprises performing an AND operation in which said control register mask and said control value are operands.

8. The method of claim 7 wherein said state save operation is an FXSAVE instruction, said FXSAVE instruction having associated with it a target address.

9. The method of claim 8 wherein said target address is an address within said memory image.

10. A machine-readable medium having stored thereon a set of instructions said set of instructions, which when executed by a processor, cause said processor to perform a method comprising:

accessing a control register mask;

adjusting a control value for a control register as a function of said control register mask to generate a masked control value;

programming said masked control value into the control register.

11. The computer-readable medium of claim 10 wherein said accessing comprises writing an initial value to at least one address within a memory image.

12. The computer-readable medium of claim 11 wherein said accessing further comprises executing a state save operation.

13. The computer-readable medium of claim 12 wherein said accessing further comprises comparing a saved value to said initial value, said saved value being stored within said memory image as a result of said execution of said state save operation.

14. The computer-readable medium of claim 13 wherein said control register mask comprises a default value if said saved value is equal to said initial value.

15. The computer-readable medium of claim 14 wherein said control register mask comprises said saved value if said saved value is not equal to said initializing value.

16. The computer-readable medium of claim 15 wherein said adjusting comprises performing an AND operation in which said control register mask and said control value are operands.

17. The computer-readable medium of claim 16 wherein said state save operation is an FXSAVE instruction, said FXSAVE instruction having associated with it a target address.

18. The computer-readable medium of claim 17 wherein said target address is an address within said memory image.

19. An apparatus comprising:

a control register comprising a plurality of bits to provide a plurality of functions;

a masking mechanism to set inactive one or more bits of a control value prior to storage of said one or more bits in the control register.

20. The apparatus of claim 19 further comprising:

a mask storage area to contain a pre-determined mask value, said mask value indicating which of said plurality of functions are available.

21. The apparatus of claim 20 wherein said mask storage area may be accessed by performing a state saving operation which saves said mask value to a memory location.

22. The apparatus of claim 21 wherein said state saving operation is an FXSAVE instruction.

23. The apparatus of claim 19 wherein said masking mechanism is a hardware masking mechanism.

24. The apparatus of claim 19 wherein said masking mechanism comprises:

a sequence of instruction to adjust a control value by saving state information including a control register value to a memory and adjusting said control register value based on a readable mask value read from the processor before restoring the state information;

execution hardware to execute the sequence of instructions.

25. A processor comprising:

a decode unit;

at least one of a plurality of registers, said at least one of a plurality of registers comprising a plurality of bits to provide a plurality of functions;

an execution unit;

an internal bus, said decoder unit, said at least one plurality of registers, said at least one execution unit being coupled by said internal bus.

26. The processor of claim 25, wherein, in response to said execution unit executing an instruction, said plurality of bits are written to a mask storage area.

27. The processor of claim 26 wherein said instruction is an FXSAVE instruction.

28. The processor of claim 27 wherein said at least one of a plurality of registers is an MXCSR register.

29. The processor of claim 28 wherein said at least one mask storage area is an MXCSR_MASK field.